Minimized Structure of NOC Router Using FPGA

Dr.Raaed Faleh Hassan, Riyam Layth Khaleel

Abstract— The work presented in this paper concerned with the design of a router as a basic component in the network on chip using Very High speed integrated circuit Hardware Description Language (VHDL). The router in this network consists of five bidirectional ports, one port for each neighbor node and the fifth port is for local processing element. The designed router deals with packet based data transfer which contains the source of data to be transferred, the desired destination and the data itself. A 25 – bit packets are used in each router port. The architecture proposed in this paper supports five connections simultaneously without any communication bottleneck, and improve the speed of communication on NOC router. Examples are presented to verify the behavior of the designed router and the simulation gives the results as expected.

Index Terms— buffer, crossbar, FPGA, NOC, packet, router, VHDL

1 INTRODUCTION

TODAY'S industry is moving towards multi core system on chip (SOC). System on Chip (SOC) is a new trend technology which includes various computer components in a single chip, such as a smartphone or wearable computer. Conventional bus based interconnection between these multi core system became impractical as the number of cores increase because of more power consuming, more size occupied and poor performance due to data queue. For providing reliable communication between these cores, Network-on-Chip (NOC) is required [1]. The use of a NOC as alternative SOC communication technology has several advantages:

- Adaptive as required from bandwidth segment wires points of view.
- Reliable performance in high loads with flexible dynamic range [2].

In recent years, many research conducted in NOC, (R. Pau) [3] proposed a router using dual crossbar to connect the input and output ports, the drawback of this router was the large number of slices required on FPGA. (Z. Link) [4] presents a new method for testing the routers in a packet switch on-chip. (I. Sen´ın) [5] suggest two types of NOC, the unidirectional and multidirectional architectures, the disadvantage of this design was poor traffic kind which the worse performance in system. (T. Karadeniz) [6] proposed improvement to the design which has been mentioned in [5] for the routing and scheduling algorithms.

(R. Sunkam) [7] propose two different approaches to maximizing throughput in NoCs First, designing efficient routing algorithms that load-balance traffic uniformly over all networks links and second, by improving the router architecture to relieve bottlenecks and improve packet-multiplexing capabilities. (M. Gibiluka) [8] presents the design and implementation of an asynchronous NoC router using a transition-signaling bundled-data protocol, but he could not synthesize a full router in time to be included in work, because the synthesis process was far more complex. (S. Murali) [2] present novel algorithmic and state-of-the-art methods to solve many of the important NoC design problems, such as core mapping, topology synthesis, crossbar sizing, resource reservation, route generation, achieving fault-tolerance and layout generation.

In this paper, a simple architecture design of router has been proposed to reduce the implementation complexity and therefore reduce the number of required logic units. Also the packet format and how choose the desired output and check collision. Finally, testing results of examples in simulation.

2 NETWORK ON CHIP ARCHITECTURE

Fig. 1 shows a network of 3×3 nodes, each node consists of three components, these are, processing element (PE), network interfacing (NI) and router (R). Each router in this network consists of five bidirectional ports, one port for each neighbor node and the fifth port is for local processing element.

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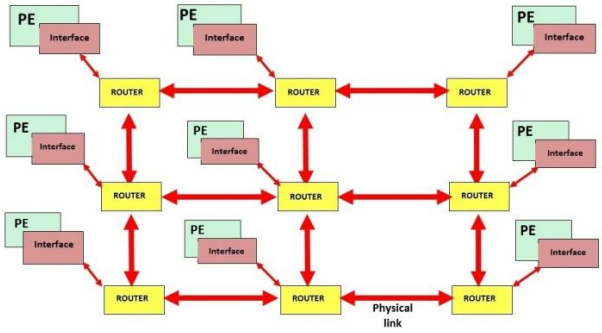


Fig. 1. 3 X 3 Network Schematic

2.1 Network Interface

(NI) is the intermediate block, between PE and router in each node that makes the logic connection between these two elements. This network interface support for sending data from PE to the router, and vice versa with low latency. The NI task is to transform the data delivered from PE to a packet form and sending to the router, as well as transforming the packet delivered from the router to a data and sending to the PE.

2.2 Processing element

(PE) which can be a processor core, a memory, DSP applications or any other processing. PE the source of the information (data packets), which is transmitted to the network [9].

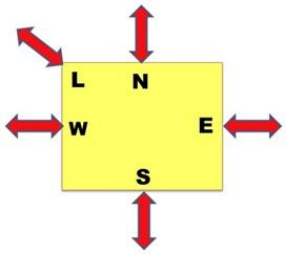
Every node in the network consists of PE, NI and Router, the node is connected with nearby nodes by the router. The router makes a decision to direct the data between nodes. A NOC is described by its routers connection topology, such as mesh, tours, tree, hypercube, etc. the interconnection structure used in this design is mesh topology NOC.

The links is composed of a set of wires that connect the nodes physically and implement the communication actually. A NOC link has two unidirectional channels in opposite directions which performing a full-duplex routers connection. The network has a uniform number of wires per channel which represent channel bit width. Routers make the routing decisions based on the routing algorithm. A routing algorithm plays important role on network' operation. The algorithm consists of a predefined procedures designed and implemented within the router, to process common statuses during the transmission of a packet, such as arriving two or more packets at the same time or competition the same channel, avoiding deadlock status, increasing the throughput, reducing the latency, etc. [10]. Sending a packet from a source PE to a destination PE, performed by forwarded it to the network according to the decision made by each router. The packet is first received by a router at input buffer. Then the decision implemented in the router which is called arbitration is responsible for directing the packet to the desired direction through a crossbar, the process repeats at each router until the packet arrives at desired destination [11].

2.3 Design of a NOC router

As mentioned previously, the backbone unit of NOC is the router. The task of the router is to determine the next hop of the received packets and direct them accordingly. In this paper the router is considered to have five bidirectional ports (North, South, East, and West) to simplify packet switching and passing, and the fifth is the entire processing element (PE) which is connected to a local router through NI. The router receives the packets from the nearby routers and its NI, and according to the address informed in each packet, it forwards the packet to NI attached to it or to another sharing routers. XY routing algorithm is considered to support the router to directs the packets to the desired direction. According to its simplicity, implemented XY routing algorithm increases router performance. The transfer of data hop by hop from source to destination is called switching mechanism. For packet-switched networks, buffering is needed, to support regular data transfers to overcome channel bottleneck and collisions. This buffering can be at the inputs or the outputs of router. Therefore, to obtain optimal performance, buffering is extremely essential. In this design, the length of buffer is equal to the packet size. The depth of buffer is five to provide input buffering, so the buffer requires five clock signals for first packet to get out of buffer [11]. Initially, the packets received by the router is stored at an input buffer of that channel. The packet is transmitted hop by hop from the source to the destination according to the routing path determined by the XY routing algorithm in each router. Routing priorities given to: Local (L), North (N), East (E), South (S), West (W) inputs. The arbiter is responsible to selects the prior input port when multiple packets arrive at the router requesting the same output port, the other channel will have to wait until it has higher priority. For each cycle the arbiter gives each channel once chance to transfer its data due to the rotating priority scheme. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffers [12]. In this paper the crossbar and arbiter has been designed logically implicitly in router to reducing the area and to relieving complexity.

Also the router has two acknowledge signals each of them is 5bit: busy-in which refers to status of ports in adjacent routers if set, this means the port is busy. Busy-out which refers to status of the router itself, it sends to adjacent router. The proposed architecture of the router is shown in Fig (2).



(a) functional view

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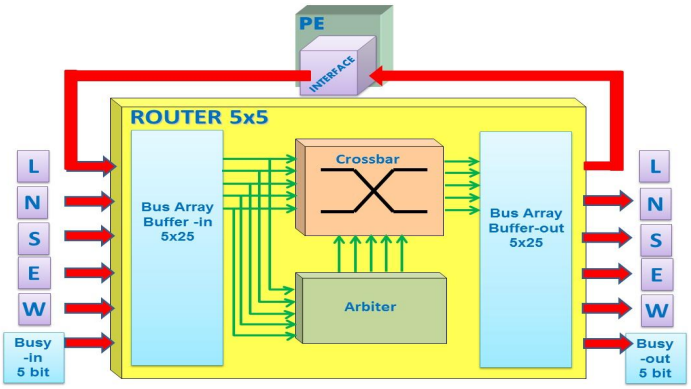

(b) architectural view
Fig. 2. Proposed Router Structure

The router puts the data in buffer (Bus array buffer-in) which connected to crossbar. The crossbar is a switch connection multiple inputs to multiple outputs in a matrix way (multiplexers). The crossbar delivered inputs to the output buffer (Bus array buffer-out). Because the crossbar can be transfers multiple data simultaneously, so the Crossbar-based systems are less expensive than bus or ring systems with equivalent performance [1].

The arbiter designed is contains buffer level1 and buffer level2 (5*25) to holds the data which in processing. Arbiter is controlled by five bit acknowledge signals, buffer level grant1 and buffer level grant2; each of them 5bit. (Buffer level used grant1) put in (busy-out) to indicate if the (buffer level1) contains data in processing. Figure (3) shows the arbiter architecture of the router.

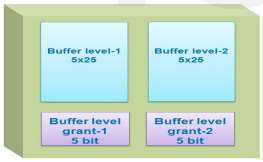

Fig. 3. The arbiter

3 Packets Architecture

Each Packet is divided to several smaller segments (flits). Flit is the basic flow control unit, each flit is several bit width. A whole packet contains 25 bit. The header length of the packet is 9 bit and the payload is 16 bit. The header contains all the requisite information to be used by the XY routing algorithm to direct a packet between two routers. Packet format proposed in this paper shown in Fig. 4.

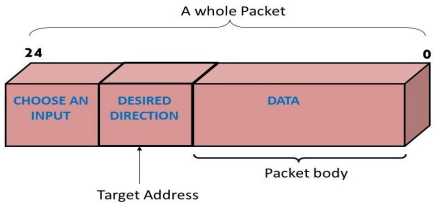

Fig. 4. Packet format

Each input has two levels of buffers. Packets held in buffers when waiting writes to same output and if the output is busy. Fig. 5. Shows the packet bits which has been used to direct the packet to proper output without collision.

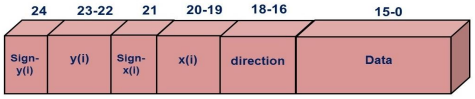

Fig. 5. Packet bits

Fig.6. is block diagram for how the used bits to direct the packet for choose the desired output and check collision.

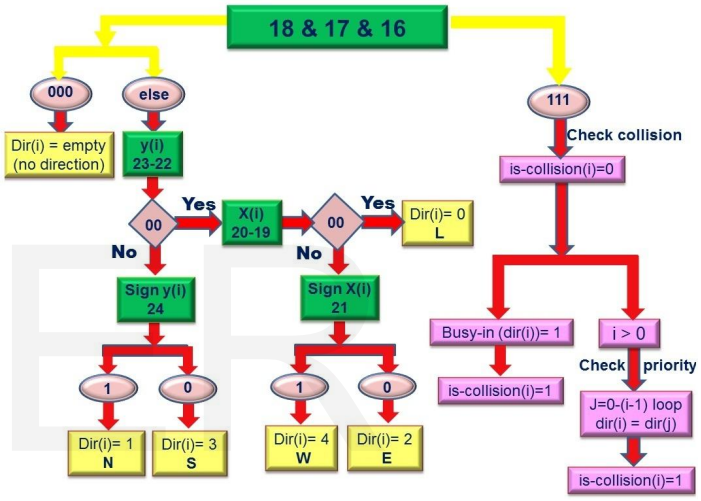

Fig. 6. Choose the desired output and check collision

4 Design Summary

The proposed router has been designed using VHDL and simulated using ISE 14.1 software package. The target device was Spartan3- XC3s5000. The device utilization summary for a 5 – ports router with 25 – bit packet is shown in Table 1.

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TABLE 1
DESIGN UTILIZATION SUMMARY

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	384	595,200	1%	
Number used as Flip Flops	384			
Number of Slice LUTs	960	297,600	1%	
Number used as logic	959	297,600	1%	
Number used as Memory	0	122,240	0%	
Number used exclusively as route-thrus	1			
Number of occupied Slices	518	74,400	1%	
Number of LUT Flip Flop pairs used	1,030			
Number of bonded IOBs	262	600	43%	
Number of RAMB36E1/FIFO36E1s	0	1,064	0%	
Number of RAMB18E1/FIFO18E1s	0	2,128	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	

5 SIMULATION RESULTS

Simulation refers to the verification of a design, its function and performance. Routing algorithm gives priority to inputs and according to that the output is assigned. If two packets want to send to the same output port, then packets on the port which has highest priority is delivered to destination first. The timing summary for functional simulation is shown in Fig. 8.

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Timing Summary:
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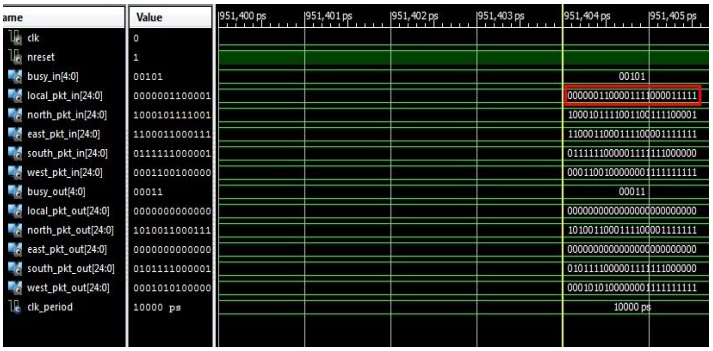
Speed Grade: -2

   Minimum period: 4.718ns (Maximum Frequency: 211.972MHz)
   Minimum input arrival time before clock: 5.044ns
   Maximum output required time after clock: 0.807ns
   Maximum combinational path delay: No path found
```

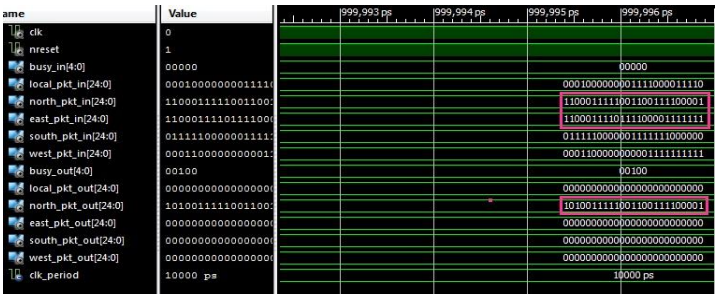
Fig.8. Timing Design Summary

As it can be seen on the simulation diagram which is shown in Fig (9 - a), the busy-in signal has a value (00101). That means the input ports (local and east) are busy and the packets in this channel still in processing, therefore no data packets in this output ports. The input ports (north, south and west) have a grant to start the data packet transfer.

According to the dynamic priority when two input packets (north and east) requested the same output direction (north), the busy-in signal (00000) for crossbar matrix is controls the output port. That means the east output port has a grant to start the data packet transfer. The data packet from east input is flow through crossbar matrix and finally the packet is being stored into buffer, and the packet in north input port has been sent. This is shown in Fig (9 - b).



(a)



(b)

Fig. 9. Output Waveform of on-chip router

4 CONCLUSION

Synchronous router architecture has been designed and implemented using VHDL. This router supports five connections at the same time without any communication bottleneck. The designed router occupies 1% from the total number of slices in the target device which is Spartan 3AN. Simulation results verifies the expected behavior of the router from dynamic routing and speed of data transfer points of view.

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